R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 2-4 and in the specification as originally filed, for example, on page 5, line 18 through page 8, line 19 and on page 9, line 4 through page 11, line 9. As such, no new matter has been introduced.

IN THE DRAWINGS

While Applicant's representative does not necessarily agree with the requirement to label FIG. 1, in order to further prosecution, FIS. 1 has been labeled "conventional." A replacement drawing sheet is submitted herewith. As such, the objection to the drawings should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1-12 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-8 and 10-20 under 35 U.S.C. §102(e) as being anticipated by Silverman, et al. (U.S. Patent No. 6,370,603, hereinafter Silverman) has been obviated by appropriate amendment and should be withdrawn.

Silverman is directed to configurable universal serial bus (USB) controller implemented on a single integrated circuit (IC) chip with media access control (MAC) (Title).

In contrast, the present invention provides (claim 1) an apparatus for coupling a peripheral device to a host comprising an interface circuit and a logic circuit. The interface circuit may be configured to (i) receive a request from the host and (ii) present a response to the request to the host. The logic circuit may be configured to (i) automatically generate the response when the request is serviceable by the logic circuit and (ii) pass (a) the request from the interface circuit to an external circuit and (b) the response from the external circuit to the interface circuit when the request is not serviceable by the logic circuit. Claims 12 and 13 include similar limitations.

Assuming, *arguendo*, the universal serial bus (USB) interface 204 of Silverman is similar to the presently claimed interface circuit, the serial interface engine (SIE) 206 of Silverman similar to the presently claimed logic circuit and the PLD 208 is similar to the presently claimed external circuit (as

suggested on page 3 of the Office Action and for which Applicant's representative does not necessarily agree), Silverman does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, Silverman appears silent regarding either the SIE 206 or the PLD 208 being able to service requests or configured to automatically generate a response to a request, as presently claimed. Silverman states that:

> According to the invention, a technique is provided for **interfacing signals to and from devices** employing disparate industry standard function. This technique is preferably implemented by combining an ASIC or other custom logic with, for example, a PLD/FPGA on a board, multichip module, or preferably on a single integrated circuit device. For a fixed-function portion, ASIC technology is suitably efficiently. PLD/FPGA technology is suitably employed for portions of the design that need to be re-configured, due to the ease and low cost of modifying their function(s). Alternatively, SRAM or Flash may be substituted for the PLD/FPGA portion (column 4, lines 15-26 of Silverman, emphasis added).

Silverman further states:

> FIG. 3 illustrates another embodiment of a configurable, single-chip USB device 302 capable of interfacing a peripheral device to the Universal Serial Bus (USB). In this embodiment, the USB controller comprises a 16-bit (e.g.) central processor 304 run by a timer (TIMER 0) 305, Flash memory 306, RAM 308, a phase lock loop (PLL) and clock generator 310, **a serial interface engine (SIE)**

> **312 (compare 206), a USB interface 314 (compare 204), and a user-programmable logic section 316 (compare 208, 208a), all interconnected as shown to provide control and data access, and USB data reception and transmission** (column 6, lines 25-35 of Silverman, emphasis added).
>
> FIG. 4 illustrates another embodiment of a configurable, single-chip USB device 402 capable of interfacing a peripheral device to the Universal Serial Bus (USB). As in the previous embodiment 300, the USB controller comprises a 16-bit (e.g.) central processor 404 (compare 304) run by two timers (TIMER 0 and TIMER 1) 405a and 405b (compare 305), flash memory 406 (compare 306), RAM 408 (compare 308), a phase lock loop (PLL) and clock generator 410 (compare 310), **a serial interface engine (SIE) 412 (compare 312), a USB interface 414 (compare 314), and a user-programmable logic section 416 (compare 316), all interconnected as shown to provide control and data access, and USB data reception and transmission** (column 6, lines 44-56 of Silverman, emphasis added).
>
> **USB transactions are automatically routed to the memory buffer 408**. The processor 404 sets up pointers and block sizes in the buffer memory 408 for the USB transactions. **Data is read from the USB interface 414**, and is **processed and packetized by the I/O processor 404** (column 7, lines 9-14 of Silverman, emphasis added).

Thus, Silverman discloses that the USB transactions are automatically routed to the memory 408 via the USB interface 414 and the SIE 412 (see FIG. 4 and column 7, lines 9-14 of Silverman). Silverman also compares the USB interface 204 and the SIE 206 with the USB interface 414 and the SIE 412, respectively. Since Silverman (i) is silent regarding either the SIE 206 or the PLD 208

being able to service requests or configured to automatically generate a response to a request, as presently claimed and (ii) compares the USB interface 204 and the SIE 206 to structures that automatically route USB transactions to a memory buffer for processing by an I/O processor, it follows that Silverman does not disclose or suggest a logic circuit coupled to an interface circuit and configured to (i) **automatically generate the response when the request is serviceable by the logic circuit** AND (ii) pass (a) the request from the interface circuit to an external circuit and (b) the response from the external circuit to the interface circuit when the request is not serviceable by the logic circuit, as presently claimed. Therefore, Silverman does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-11 and 14-20 depend, either directly or indirectly, from claims 1 and 13 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 9 under 35 U.S.C. §103(a) as being unpatentable over Silverman has been obviated by appropriate amendment and should be withdrawn.

Claim 9 depends directly from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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